EE/CprE/SE 492 BIWEEKLY REPORT 6

Date: ***November 9th, 2023 – November 22nd, 2023***

Group number: ***sddec23-08***

Project title: ***ReRAM Compute ASIC Fabrication***

Client &/Advisor: ***Henry Duwe & Cheng Wang***

Team Members/Role:

- ***Josh Thater - Mixed Signal Designer***
- ***Matt Ottersen - VLSI Designer***
- ***Aiden Petersen - Digital Designer***
- ***Regassa Dukele - VLSI Designer***

Biweekly Summary

Over the past couple of weeks, we have worked towards the completion of our project. The first part of this was completing schematic-level simulations on our top-level design. When doing read/MAC operations, we ran into some trouble with the 0.2 V read voltage and the 0.4 MAC voltage being applied across the ReRAM. The problem was on the max extreme for the 0.2 V and the minimum extreme for 0.4 V, the output voltage was too close. Essentially, what this could mean is that we could get false positives if a single cell in a column is in an LRS.

So, to counteract this, we decided to create two separate “computational crossbars.” One would have a TIA size of the 0.2 V, and the other would be the same design, just with a TIA sized for 0.4 V. We did this so we could reasonably guarantee that we could output “high” whenever 1 ReRAM cell or more were in a LRS. With this updated design, we went to work on simulating the two. For each, we tested different states of the ReRAM, such as 8 in an LRS, 0 in an LRS, 1 in an LRS and 7 in an HRS, etc.

Along with this, we also tried to do some accuracy/error testing as well. For these tests, we applied different corners, such as TT, FF, SS, FS, and SF, to each case to ensure that everything would still work as expected. We also changed the conductance of the LRS from a minimum value of 80 uS to 100 uS to make sure that everything would work at both extremes. For all of our testing, we created a table to record the results. After running through all the

testing, we verified that everything was still behaving as expected. A figure of the tables we recorded is seen below.

At 0.2 V, 80 uS

# of cells "on"	# of cells "off"	TEST	BL_In (V)	SL_In (V)	InvOut (V)	Vout (V)
0	8	TT	0.1879	0.0592	0.4692	0.0057
0	8	SS	0.1847	0.0578	0.4557	0.0039
0	8	FF	0.1901	0.0602	0.4795	0.0077
0	8	FS	0.1843	0.0595	0.4509	0.0039
0	8	SF	0.1898	0.0583	0.4775	0.0075
# of cells "on"	# of cells "off"	TEST	BL_In (V)	SL_In (V)	InvOut (V)	Vout (V)
1	7	TT	0.1804	0.1203	0.7049	1.784
1	7	SS	0.1749	0.1147	0.7064	1.787
1	7	FF	0.1846	0.1245	0.7057	1.778
1	7	FS	0.1746	0.1143	0.7165	1.789
1	7	SF	0.1844	0.1247	0.6944	1.775
# of cells "on"	# of cells "off"	TEST	BL_In (V)	SL_In (V)	InvOut (V)	Vout (V)
8	0	TT	0.1783	0.1666	0.772	1.789
8	0	SS	0.1715	0.1601	0.7763	1.792
8	0	FF	0.1846	0.1243	0.7057	1.778
8	0	FS	0.1746	0.1143	0.7165	1.789
8	0	SF	0.1844	0.1247	0.6944	1.775

At 0.4 V, 80 uS

# of cells "on"	# of cells "off"	TEST	BL_In (V)	SL_In (V)	InvOut (V)	Vout (V)
0	8	TT	0.3694	0.7192	0.429	0.0226
0	8	SS	0.3613	0.7045	0.4154	0.01328
0	8	FF	0.3749	0.7293	0.4394	0.03421
0	8	FS	0.3602	0.7223	0.4208	0.01415
0	8	SF	0.3754	0.7062	0.4421	0.03053
# of cells "on"	# of cells "off"	TEST	BL_In (V)	SL_In (V)	InvOut (V)	Vout (V)
1	7	TT	0.3436	0.1818	0.7345	1.788
1	7	SS	0.3282	0.1684	0.7314	1.79
1	7	FF	0.3543	0.1919	0.7333	1.784
1	7	FS	0.3258	0.1668	0.735	1.792
1	7	SF	0.3555	0.1928	0.7255	1.781
# of cells "on"	# of cells "off"	TEST	BL_In (V)	SL_In (V)	InvOut (V)	Vout (V)
8	0	TT	0.3315	0.2987	0.8189	1.793
8	0	SS	0.3122	0.2796	0.8225	1.796
8	0	FF	0.3447	0.3119	0.8095	1.791
8	0	FS	0.3091	0.2765	0.8297	1.796
8	0	SF	0.3462	0.3134	0.7975	1.789

At 0.2 V, 100 uS

# of cells "on"	# of cells "off"	TEST	BL_In (V)	SL_In (V)	InvOut (V)	Vout (V)
0	8	TT	0.1879	0.0592	0.4692	0.0057
0	8	SS	0.1847	0.0578	0.4557	0.0039
0	8	FF	0.1901	0.0602	0.4795	0.0077
0	8	FS	0.1843	0.0595	0.4509	0.0039
0	8	SF	0.1898	0.0583	0.4775	0.0075
# of cells "on"	# of cells "off"	TEST	BL_In (V)	SL_In (V)	InvOut (V)	Vout (V)
1	7	TT	0.1799	0.128	0.7177	1.786
1	7	SS	0.1742	0.1221	0.7217	1.788
1	7	FF	0.1842	0.1323	0.07172	1.78
1	7	FS	0.1739	0.1216	0.7316	1.79
1	7	SF	0.184	0.1325	0.7058	1.778
# of cells "on"	# of cells "off"	TEST	BL_In (V)	SL_In (V)	InvOut (V)	Vout (V)
8	0	TT	0.1782	0.1688	0.7741	1.79
8	0	SS	0.1714	0.1632	0.7786	1.79
8	0	FF	0.1824	0.1732	0.7636	1.78
8	0	FS	0.1704	0.1613	0.7853	1.793
8	0	SF	0.1826	0.1736	0.7508	1.784

At 0.4 V, 100 uS

# of cells "on"	# of cells "off"	TEST	BL_In (V)	SL_In (V)	InvOut (V)	Vout (V)
0	8	TT	0.3694	0.7192	0.429	0.0226
0	8	SS	0.3613	0.7045	0.4154	0.01328
0	8	FF	0.3749	0.7293	0.4394	0.03421
0	8	FS	0.3602	0.7223	0.4208	0.01415
0	8	SF	0.3754	0.7062	0.4421	0.03053
# of cells "on"	# of cells "off"	TEST	BL_In (V)	SL_In (V)	InvOut (V)	Vout (V)
1	7	TT	0.3415	0.1997	0.753	1.794
1	7	SS	0.3253	0.1851	0.7502	1.796
1	7	FF	0.3526	0.2105	0.7503	1.792
1	7	FS	0.3228	0.1831	0.7569	1.796
1	7	SF	0.3538	0.2116	0.7403	1.791
# of cells "on"	# of cells "off"	TEST	BL_In (V)	SL_In (V)	InvOut (V)	Vout (V)
8	0	TT	0.331	0.304	0.8207	1.797
8	0	SS	0.3116	0.285	0.825	1.798
8	0	FF	0.3443	0.3176	0.8125	1.795
8	0	FS	0.3084	0.2819	0.8349	1.798
8	0	SF	0.3458	0.3192	0.8003	1.794

Figure 1: Table of Testing Results

Once we verified that our top level was able to do Read/MAC operations, we moved to create the layouts. Due to changing the schematic once again, we had to go through and change some of the layouts that were already created. We also had to create new ones for the 8 select line outputs. We had to create two different versions of this 8-line select output - one sized for 0.2 V and one sized for 0.4 V. Once all this was created, we then hooked everything together: 8-line bit input, 8-line word line input, 8-line select input, 8 line select output, and the 8x8 ReRAM crossbar. Once this was all hooked up for both crossbar designs, we then stuck it in the harness and manually hooked up our designs to the different pins.

Once we had hooked our “computational crossbars,” we also placed different individual components into the layout area and hooked them up to IO pins so we could individually test them out. We did this so we could check to see if our components work individually in case our design does not work once fabricated. The figure on the following page demonstrates the final layout, all hooked up to the harness. The 0.2 V crossbar is seen in the bottom left, the 0.4 crossbar is seen in the bottom right. The individual components are hard to see, but they are spread out all around the edges of the harness.

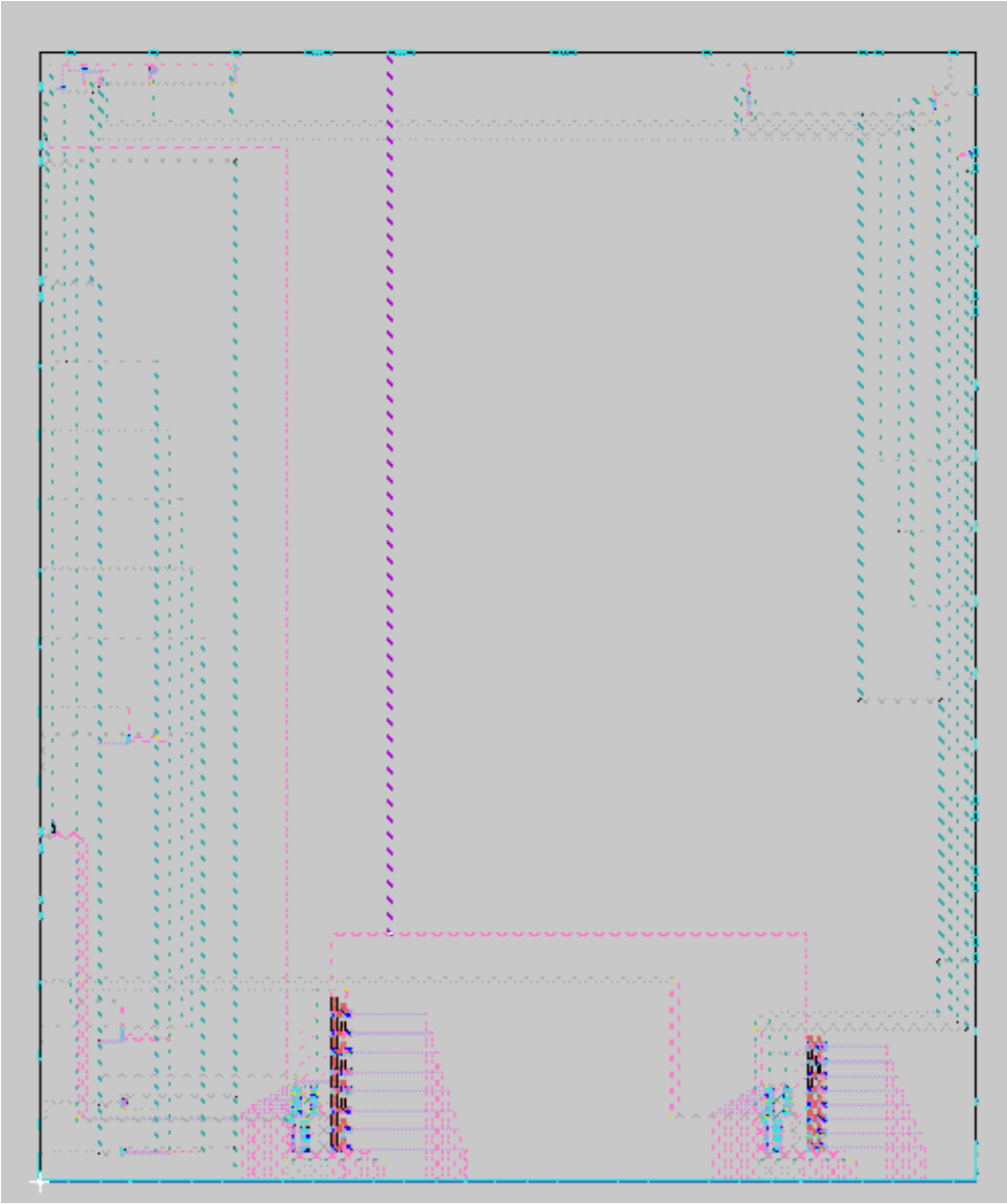

Figure 2: Final Layout Hooked up to Harness

With all of that done, we continued to work on the documentation side of our project. This included finishing up the “tutorial documentation” and beginning to create the bring-up plan for our design. We also began work on updating the final report, poster, and presentation for this class. On the digital side, we did some more testing of the quantization model to back up our claims for using the threshold of 1 for our design. We also updated the drives to match the updated schematic and to include the second ReRAM crossbar. Finally, we are collecting all

our components and all of their files into a single GitHub repository so that future work can be done on our designs.

Past Weeks Accomplishments

- Joshua Thater
    - Helped with simulating the top level of our design
        - Updated schematic/design so that we could do 0.2 V and 0.4 V read/MAC
    - Helped record test data for top-level design
    - Tweaked 8-line bit input layout and 8-line select layout to match the new schematic
    - Created 2 different versions of the 8-line select output
        - One for 0.2 V and one for 0.4 V
    - Hooked up all parts of the layout design together
    - Connected both the 0.2 V and 0.4 V “computational crossbar” to the harness pins
    - Connected up all of the individual components to analog IO pins on the harness
    - Finished up the “tutorial documentation”
        - This ended up being 75 pages long:
            - https://docs.google.com/document/d/1B99C8Lep7ePQcIg7qA_el3WZ6WbXc6nguQJsJVFJDbw/edit?usp=sharing
    - Collected all components and their files and put them all into a single GitHub repository
- Aiden Petersen
    - Developed simulations to ensure the functionality of quantized inputs
        - Analyzed the performance degradation by changing using the absolute difference
    - Wrote the documentation for the digital design flow
    - Updated drivers because of design changes
- Matt Ottersen
    - Worked on sizing the TIA for 0.2V and 0.4V 8-line select output
    - Worked on resizing ADC for lower threshold
    - Ran simulations and collected data
- Regassa Dukele
    - Helped with simulating design
    - Recorded simulation data in the table for different tests
    - Helped come up with new schematic design

Pending Issues

- Finishing up the final report, poster, and IRP presentation
- How to “hand off” the project to the next senior design team

Individual Contributions

Team Member	Individual Contributions	BIweekly Hours	Total Hours
Joshua Thater	Helped with schematic testing, tweaked old layouts, and created new ones. Hooked up all components/top-level design in harness. Finished “tutorial documentation.” Collected all components into a single repository.	35	195
Aiden Petersen	Performance analysis for quantization, writing digital design documentation, and updating drivers.	15	125
Matt Ottersen	Sized components and ran simulations	14	124
Regassa Dukele	Helped with creation of new schematic and recording testing results	14	127

Plans for the Upcoming Weeks

- Joshua Thater
    - Help with creating the poster and final presentation
    - Finish/edit the final report
    - Do a write-up on handing off the project to the next team
- Aiden Petersen
    - Final presentation, posters, etc.
    - Accuracy analysis of framework in tensorflow.
- Matt Ottersen
    - Work on final presentation and poster
    - Work on bring up plan
- Regassa Dukele
    - Help with creation of poster and final presentation
    - Edit final report
    - Assist with bring-up plan